USSN 09/964,472
Art Unit: 2812

In the claims:

Please amend the claims as follows:

1(currently amended). A ~~method~~ manufacturing process for ~~of~~ making various high-voltage bipolar/CMOS/DMOS (BCD) integrated circuits of different type using a limited number of different mask steps, said ~~method~~ process comprising:

(a) predefining a set of mask steps, each mask step comprising performing an associated activity ~~using~~ through a separate mask distinct from the respective masks associated with the other mask steps of said set of mask steps ~~to perform an associated activity~~;

(b) identifying a plurality of specific sequences of mask steps from said predefined set, each specific sequence being associated with the manufacture of one or more specific integrated circuits;

(c) selecting a specific integrated circuit to manufacture;

(d) selecting one of said specific sequences of mask steps from said predefined set of mask steps as a selected specific sequence to manufacture said specific integrated circuit;

(e) providing a starting material selected from the group consisting of: a p-type bulk substrate, ~~or~~ and a p-type epitaxial layer over a P^+ bulk substrate~~f p-type material~~; and

(f) performing said selected sequence of mask steps on said starting material in numerical order to make said selected specific integrated circuit; and

said predefined set of mask steps consisting essentially of:

(1) a first mask step wherein ~~a mask is used to form at least one~~ an n-type implant is performed in ~~N-well in~~ said p-type material to form an N-well with the aid of a mask identified as an N-well mask;

(2) a second mask step wherein ~~mask is used to form~~ an active region is formed by etching through an oxidation layer with the aid of a mask identified as an active region mask;

(3) a third mask step wherein ~~a mask is used to form~~ a p-type field region is formed by performing a p-type implant with the aid of a mask identified as a P-field mask;

(4) a fourth mask step wherein ~~a mask is used to form~~ a gate oxide is etched with the aid of a mask identified as a gate oxide mask;

(5) a fifth mask step wherein ~~a mask is used to carry out~~ a p-type implantation is carried out with the aid of a mask identified as a thin gate oxide mask;

(6) a sixth mask step wherein ~~mask is used to form~~ polysilicon gate regions are etched with the aid of a mask identified as a polysilicon gate patterning mask;

(7) a seventh mask step wherein ~~a mask is used to form~~ a p-base region is formed by p-type implantation with the aid of a mask identified as a p-base mask;

(8) an eighth mask step wherein ~~a mask used to form~~ a N-extended region is formed by N-type implantation with the aid of a mask identified as an N-extended region mask;

(9) a ninth mask step ~~step~~ wherein ~~a mask is used to form~~ a p-top region is formed by p-type implantation with the aid of a mask identified as a P-top mask;

(10) a tenth mask step wherein ~~a mask is used to carry out~~ an N+ implantation is carried out with the aid of a mask identified as an N^+ implant mask;

(11) an eleventh mask step wherein ~~a mask is used to carry out~~ a P^+ implantation is carried out with the aid of a mask identified as a P^+ implant mask;

(12) a twelfth mask step wherein ~~a mask is used to form~~ contacts are etched with the aid of a mask identified as a contact mask;

(13) a thirteenth mask step wherein ~~a mask is used in the deposition of~~ a deposited first metal layer is etched with the aid of a mask identified as a first metal mask;

(14) a fourteenth mask step wherein ~~a mask is used to form~~ vias are etched in underlying material with the aid of a mask identified as a vias mask;

(15) a fifteenth mask step wherein ~~a mask is used in the deposition of~~ a deposited second metal layer is etched with the aid of a mask identified as a second metal mask; and

(16) a sixteenth mask step wherein ~~a mask is used in the formation of~~ a passivation layer is etched with the aid of a mask identified as a passivation mask; and

wherein said selected specific sequence consists of at least said mask steps 1 to 3, 5, 6, and 10 to 16 and at least one of said mask steps 4, 7, 8, and 9 depending on the type of said selected specific integrated circuit.

2.(currently amended) ~~A method~~The process as claimed in claim 1, wherein said selected sequence comprises mask steps 1, 2, 3, 5, 6, 8, 10, 11, 12, 13, 14, 15, and 16.

3.(currently amended) ~~A method~~The process as claimed in claim 1, wherein said selected sequence comprises mask steps 1, 2, 3, 5, 6, 9, 10, 11, 12, 13, 14, 15, and 16.

4.(currently amended) ~~A method~~The process as claimed in claim 1, wherein said selected sequence comprises mask steps 1, 2, 3, 5, 6, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

5.(currently amended) ~~A method~~The process as claimed in claim 1, comprising mask steps 1, 2, 3, 5, 6, 7, 10, 11, 12, 13, 14, 15, and 16.

6.(currently amended) ~~A method~~The process as claimed in claim 1, wherein said selected specific sequence comprises mask steps 1, 2, 3, 5, 6, 7, 8, 10, 11, 12, 13, 14, 15, and 16.

7.(currently amended) ~~A method~~The process as claimed in claim 1, wherein said selected specific sequence comprises mask steps 1, 2, 3, 5, 6, 7, 9, 10, 11, 12, 13, 14, 15, and 16.

8.(currently amended) ~~A method~~The process as claimed in claim 1, wherein said selected specific sequence comprises mask steps 1, 2, 3, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

9.(currently amended) ~~A method~~The process as claimed in claim 1, wherein said selected specific sequence comprises mask steps 1, 2, 3, 4, 5, 6, 10, 11, 12, 13, 14, 15, and 16.

10.(currently amended) ~~A method~~The process as claimed in claim 1, wherein said selected sequence comprises mask steps 1, 2, 3, 4, 5, 6, 9, 10, 11, 12, 13, 14, 15, and 16.

11.(previously amended) ~~A method~~The process as claimed in claim 1, wherein said selected specific sequence comprises mask steps 1, 2, 3, 4, 5, 6, 8, 10, 11, 12, 13, 14, 15, and 16.

12.(currently amended) ~~A method~~The process as claimed in claim 1, wherein said selected sequence comprises mask steps 1, 2, 3, 4, 5, 6, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

13.(currently amended) ~~A method~~The process as claimed in claim 1, wherein said selected specific sequence comprises mask steps 1, 2, 3, 4, 5, 6, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

14.(currently amended) ~~A meth~~The process~~ed~~ as claimed in claim 1, wherein said selected sequence comprises mask steps 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, and 16.

15.(currently amended) ~~A method~~The process as claimed in claim 1, wherein said selected specific sequence comprises mask steps 1, 2, 3, 4, 5, 6, 7, 8, 10, 11, 12, 13, 14, 15, and 16.

16.(currently amended) ~~A method~~The process as claimed in claim 1, wherein said selected specific sequence comprises mask steps 1, 2, 3, 4, 5, 6, 7, 10, 11, 12, 13, 14, 15, and 16.

17.(currently amended) ~~A method~~The process as claimed in claim 1, wherein said selected specific sequence comprises mask steps 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, and 16.

18(cancelled)

19(cancelled)

20.(Currently amended) ~~A method~~ The process as claimed in claim 1, wherein:

a) mask step1 comprises the sub-steps of:

(i) using P- bulk Silicon as a starting material;

(ii) performing an initial oxidation;

(iii) performing a photolithographic step;

(iv) performing an N-Type Implant to create said N-Well; and

(v) performing a diffusion;

b) mask step 2 comprises the sub-steps of:

(i) performing and oxide etch;

(ii) performing an oxidation;

(iii) performing a silicon nitride deposition;

(iv) performing a photolithographic step; and

(v) performing a nitride etch;

c) mask step 3 comprises the sub-steps of:

(i) performing a photolithographic step;

(ii) performing a P-Type Implant;

(iii) performing a blanket N-Type Implant;

(iv) performing an oxidation step to form a field oxide;

(v) performing a nitride etch;

(vi) performing an oxide etch; and

(iv) performing an oxidation to form a pre-gate oxide;

d) mask step 4 comprises the sub-steps of:

(i) performing an oxide etch;

(ii) performing an oxidation the gate oxide; and

(ii) performing a photolithographic step;

e) mask step 5 comprises the sub-steps of:

(i) performing an oxide etch;

(ii) performing an oxidation to form said thin gate oxide;

(iii) performing a photolithographic step;

(iv) performing a P-Type Implant;

f) mask step 6 comprises the sub-steps of:

(i) performing polysilicon gate deposition;

(ii) performing polysilicon doping;

(iii) performing a photolithographic step;

(iv) performing a polysilicon etch;

g) mask step 7 comprises the sub-steps of:

(i) performing a photolithographic step;

(ii) performing a P-type implant to form the P-base;

h) mask step 8 comprises the sub-steps of:

(i) performing a photolithographic step;

(ii) performing an N-type implant;

i) mask step 9 comprises the sub-steps of:

(i) performing a photolithographic step;

(ii) performing a P-type implant;

(j) mask step 10 comprises the sub-steps of:

(i) performing an oxidation and diffusion step;

(ii) performing a polysilicon oxidation;

(iii) performing a photolithographic step; and

(iv) performing an N-type implant to create said N^+ implant region;

(k) mask step 11 comprises the sub-steps of:

(i) performing a photolithographic step; and

(ii) performing a P-type implant to create said P^+ implant region;

(l) mask step 12 comprises the sub-steps of:

(i) performing a SG/PSG/SOG deposition;

(ii) performing a diffusion step; and

(iii) performing a photolithographic step; and

(iv) performing a contact etch;

(m) mask step 13 comprises the sub-steps of:

(i) performing a Ti/TiN deposition with oxidation;

(ii) performing an aluminum alloy deposition;

(iii) performing a photolithographic step;

(iv) performing a metal etch; and

(v) performing dielectric and SOG deposition;

(n) mask step 14 comprises the sub-steps of:

(i) performing a photolithographic step; and

(ii) etching said vias; and

(o) mask step 15 comprises the sub-steps of:

(i) performing Ti/TiN deposition with oxidation;

(ii) performing an aluminum alloy deposition;

(iii) performing a photolithographic step;

(iv) performing a metal etch;

(v) performing an oxide/nitride deposition;

(vi) performing a photolithographic step; and

(vii) performing an oxide etch.

21(new). A manufacturing process for making various high-voltage bipolar/CMOS/DMOS (BCD) integrated circuits comprising:

(a) providing a starting material selected from the group consisting of: a p-type bulk substrate, and a p-type epitaxial layer over a P^+ bulk substrate; and

(b) performing a sequence of mask steps on said starting material, each mask step comprising performing an associated activity through a separate mask distinct from the respective masks associated with other mask steps of, wherein said sequence of mask steps comprises:

(1) a first mask step wherein an n-type implant is performed in said p-type material to form an N-well with the aid of a mask identified as an N-well mask;

(2) a second mask step wherein an active region is formed by etching through an oxidation layer with the aid of a mask identified as an active region mask;

(3) a third mask step wherein a p-type field region is formed by performing a p-type implant with the aid of a mask identified as a P-field mask;

(4) a fourth mask step wherein a gate oxide is etched with the aid of a mask identified as a gate oxide mask;

(5) a fifth mask step wherein a p-type implantation is carried out with the aid of a mask identified as a thin gate oxide mask;

(6) a sixth mask step wherein gate regions are etched with the aid of a mask identified as a polysilicon gate patterning mask;

(7) a seventh mask step wherein an N+ implantation is carried out with the aid of a mask identified as an N^+ implant mask;

(8) an eighth mask step wherein a P^+ implantation is carried out with the aid of a mask identified as a P^+ implant mask;

(9) a ninth mask step wherein contacts are etched with the aid of a mask identified as a contact mask;

(10) a tenth mask step wherein a deposited first metal layer is etched with the aid

of a mask identified as a first metal mask;

(11) an eleventh mask step wherein vias are etched in underlying material with the aid of a mask identified as a vias mask;

(12) a twelfth mask step wherein a deposited second metal layer is etched with the aid of a mask identified as a second metal mask; and

(13) a thirteenth mask step wherein a passivation layer is etched with the aid of a mask identified as a passivation mask.

22. The process of claim 21, further comprising a further distinct and separate intermediate mask step between said sixth and seventh recited mask steps, said further distinct and separate intermediate mask step comprising forming a p-top region by p-type implantation with the aid of a mask identified as a P-top mask.